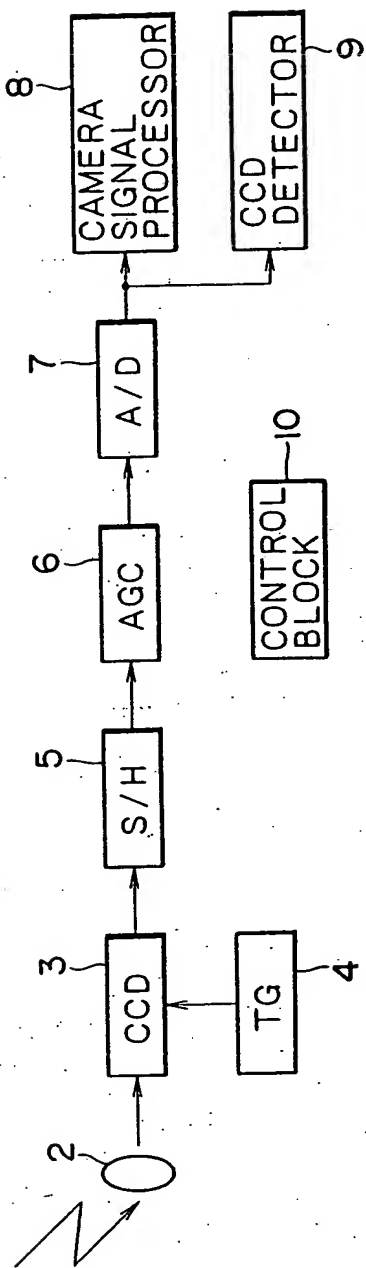


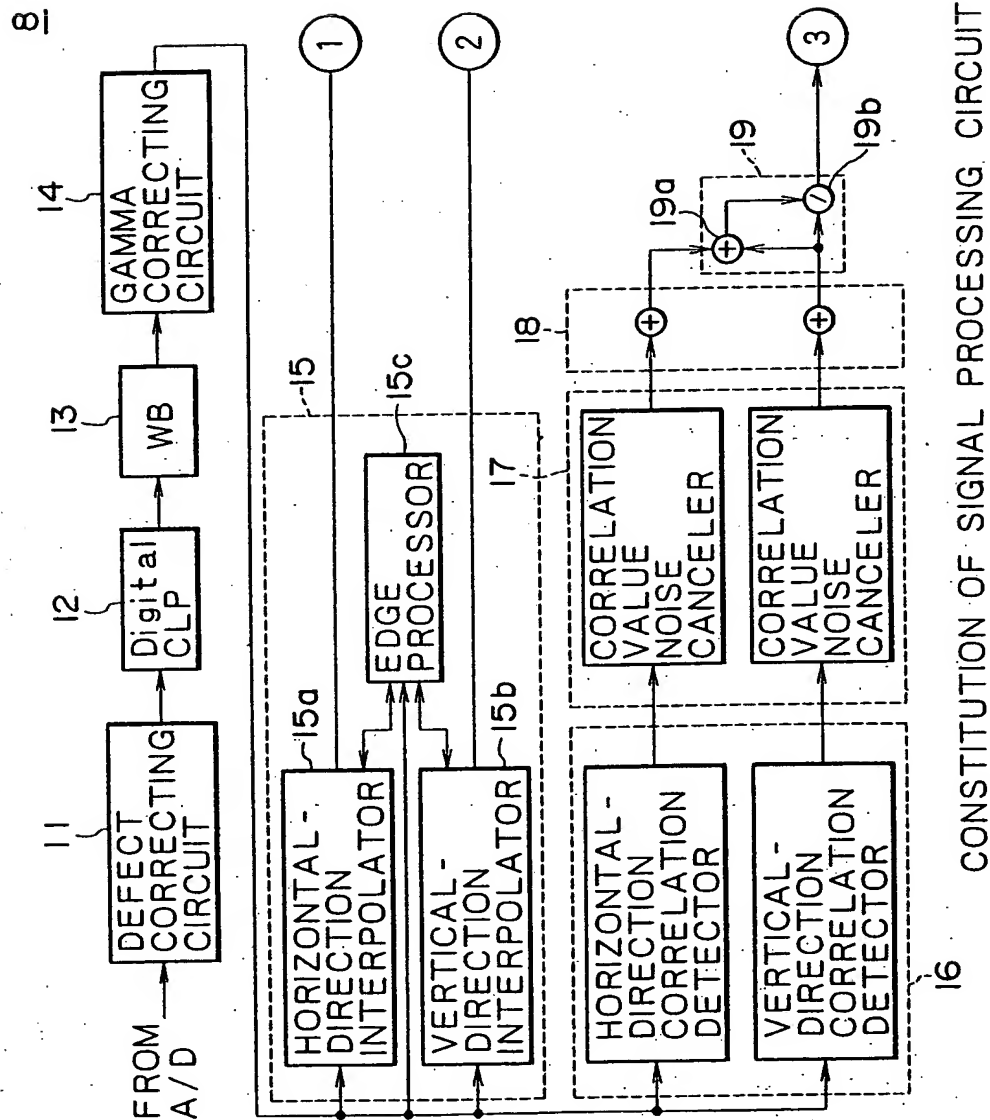
FIG. 1

1



CONSTITUTION OF CAMERA APPARATUS

# FIG. 2A



CONSTITUTION OF SIGNAL PROCESSING CIRCUIT

FIG. 2B

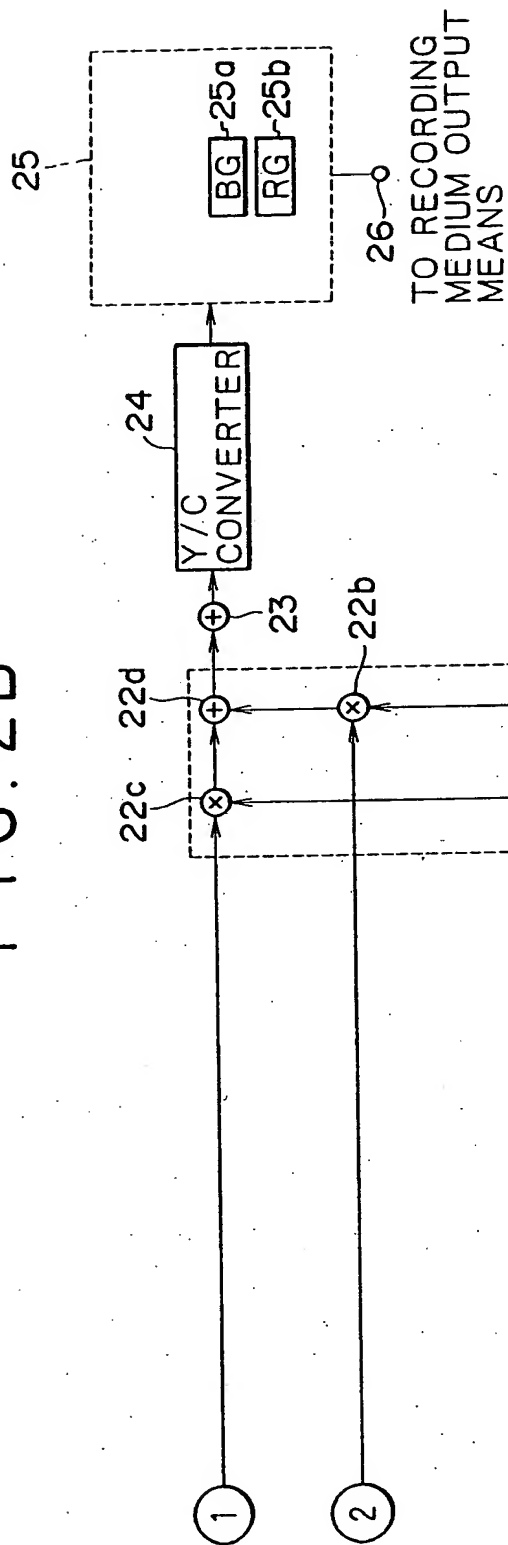
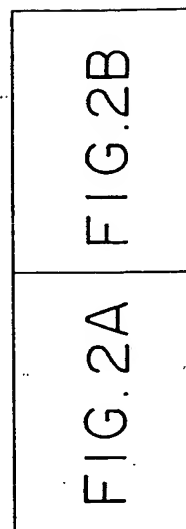


FIG. 2



# FIG. 3

0h	G 00	R 01	G 02	R 03	G 04	
1h	B 10	G 11	B 12	G 13	B 14	
2h	G 20	R 21	G 22	R 23	G 24	
3h	B 30	G 31	B 32	G 33	B 34	
4h	G 40	R 41	G 42	R 43	G 44	

## ARRANGEMENT OF PIXEL DATA

Figure 1 is a block diagram of a digital circuit for calculating the sum of squares of two 24-bit numbers. The circuit includes a 24-bit input 'From 2hDL 30', four 24-bit registers (31a, 31b, 31c, 31d), and a series of adders (32a, 32b, 32c, 32d) and shifters (33a, 33b, 33c, 33d). The adders perform operations like (X6), >>1(1/2), and >>3(1/8). The shifters perform operations like <<2, <<1, and >>1(1/2). The final output is 'LINE B/XR' and 'DOT R/XB'.

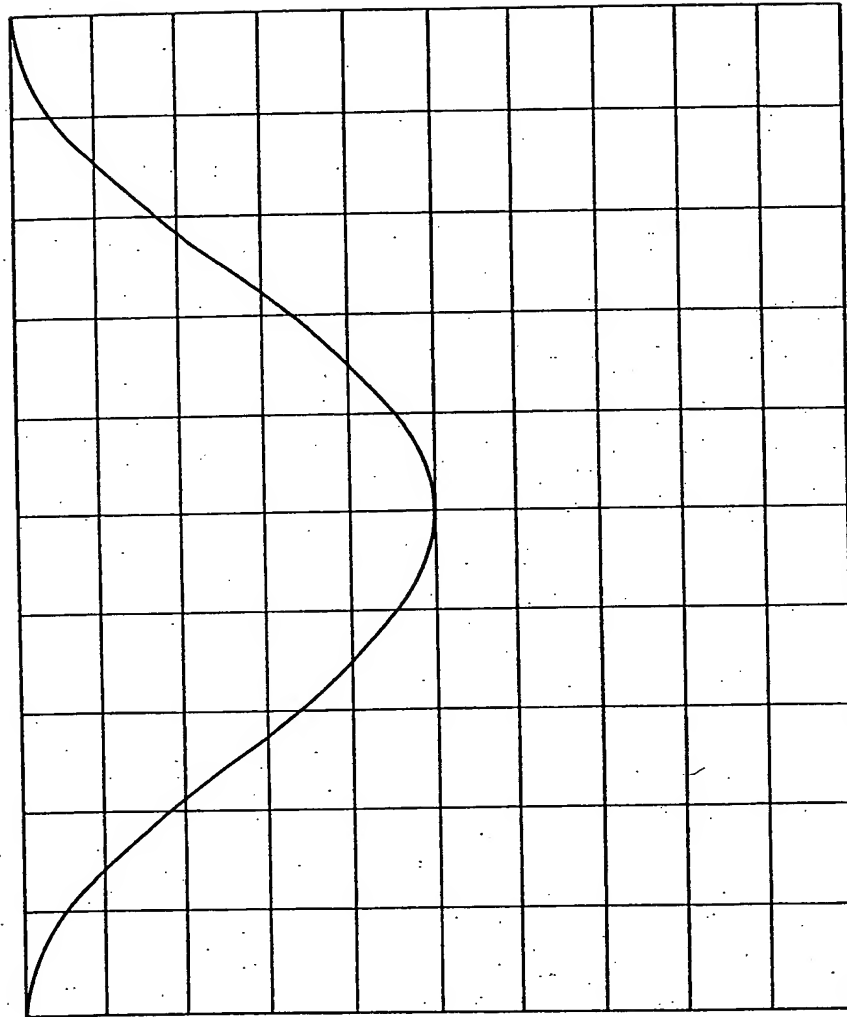
# CONSTITUTION OF HORIZONTAL-DIRECTION INTERPOLATOR

# FIG. 5

G 00		G 02		G 04	
	G 11		G 13		
G 20		G 22		G 24	
	G 31		G 33		
G 40		G 42		G 44	

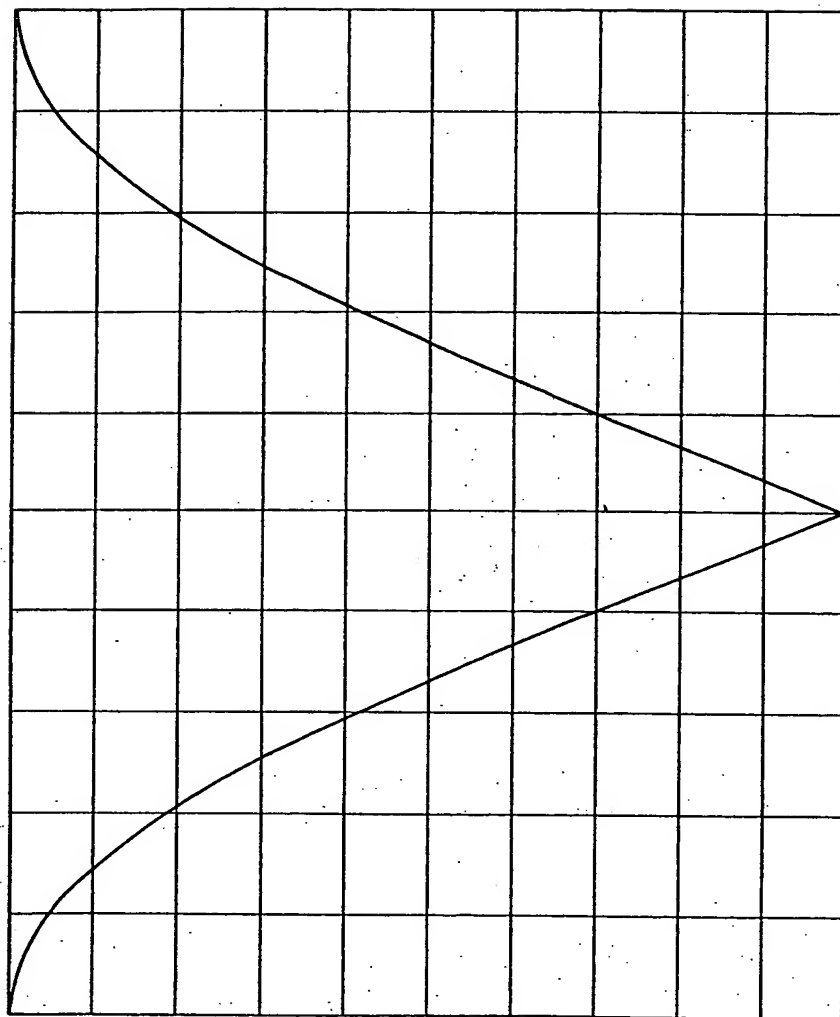
ARRANGEMENT OF PIXEL DATA

FIG. 6



FREQUENCY CHARACTERISTIC OF LPF

FIG. 7



FREQUENCY CHARACTERISTIC OF LPF

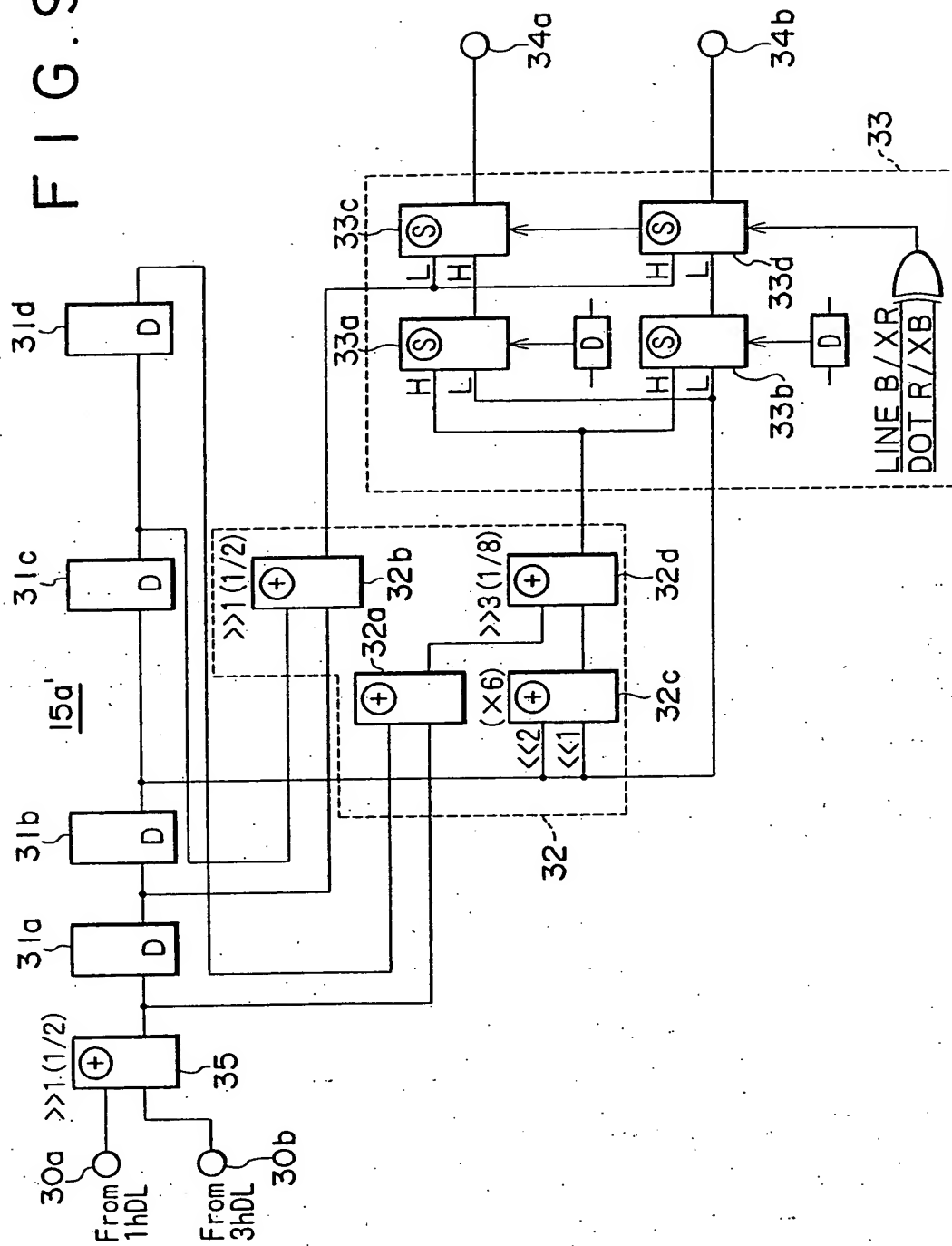


FIG. 8

G 00'	G 01'	G 02'	G 03'	G 04'	
G 10'	G 11'	G 12'	G 13'	G 14'	
G 20'	G 21'	G 22'	G 23'	G 24'	
G 30'	G 31'	G 32'	G 33'	G 34'	
G 40'	G 41'	G 42'	G 43'	G 44'	

INTERPOLATED PIXEL DATA

FIG. 9



CONSTITUTION OF HORIZONTAL-DIRECTION INTERPOLATOR

# FIG. 10

0h					
1h	B 10		B 12		B 14
2h					
3h	B 30		B 32		B 34
4h					

ARRANGEMENT OF PIXEL DATA

# FIG. 11

B 10		B 12		B 14	
B' 20		B' 22		B' 24	
B 30		B 32		B 34	

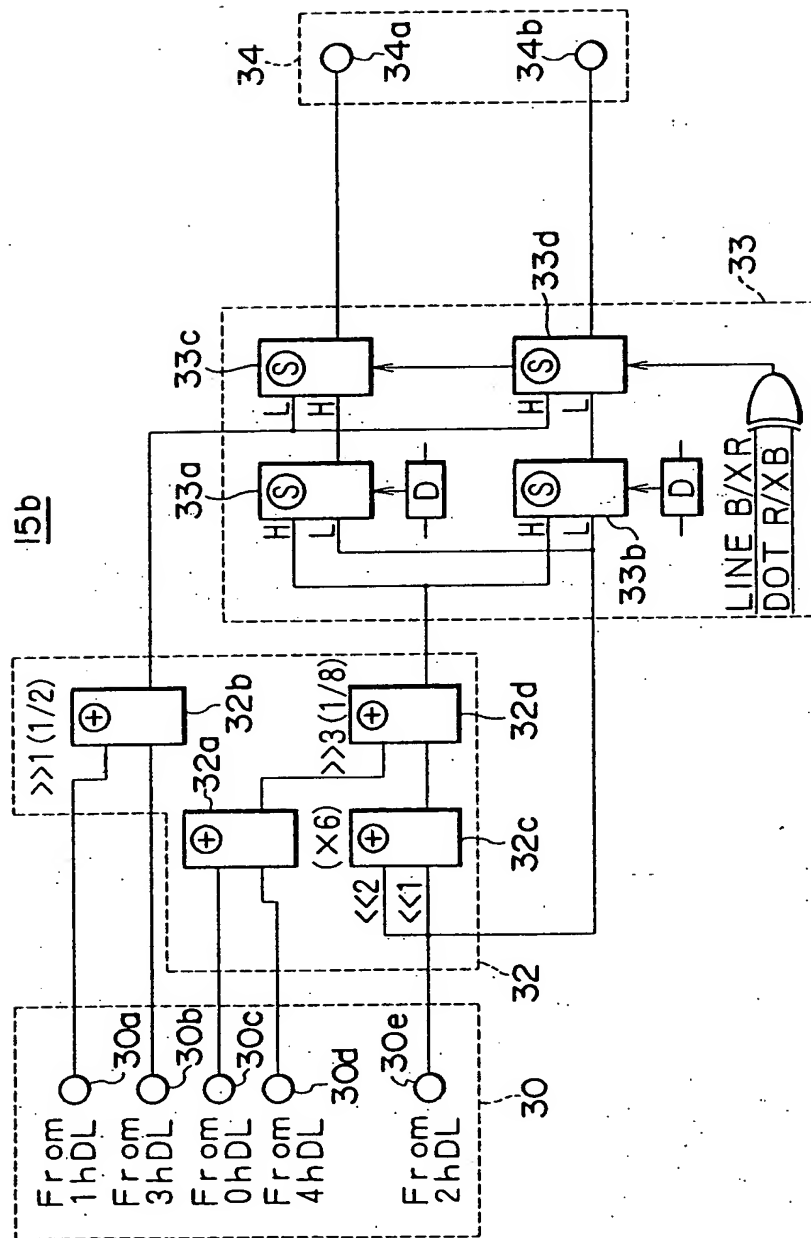
ARRANGEMENT OF PIXEL DATA

FIG. 12

B 00'	B 01'	B 02'	B 03'	B 04'	
B 10'	B 11'	B 12'	B 13'	B 14'	
B 20'	B 21'	B 22'	B 23'	B 24'	
B 30'	B 31'	B 32'	B 33'	B 34'	

INTERPOLATED PIXEL DATA

# FIG. 13



CONSTITUTION OF VERTICAL-DIRECTION INTERPOLATOR

# FIG. 14

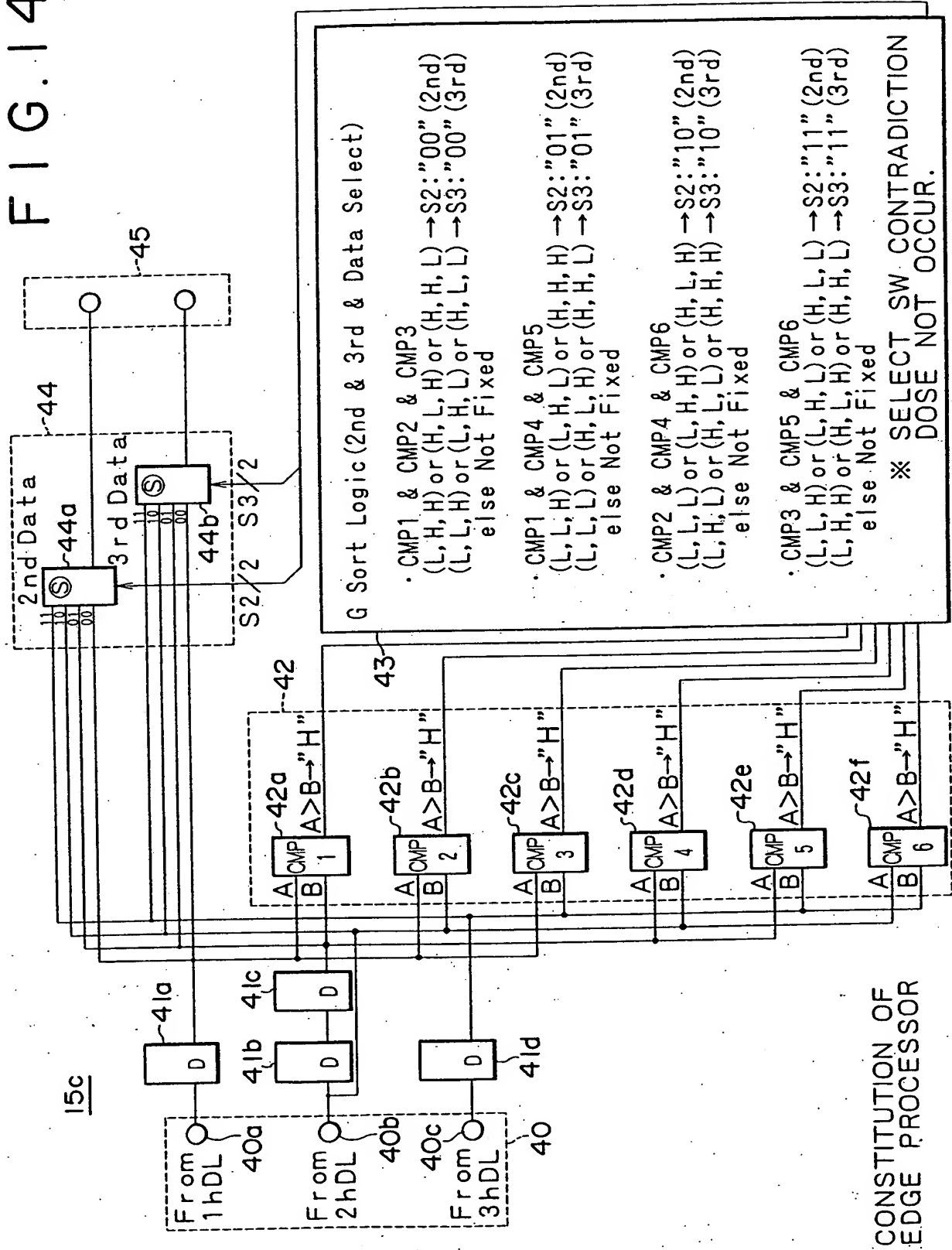
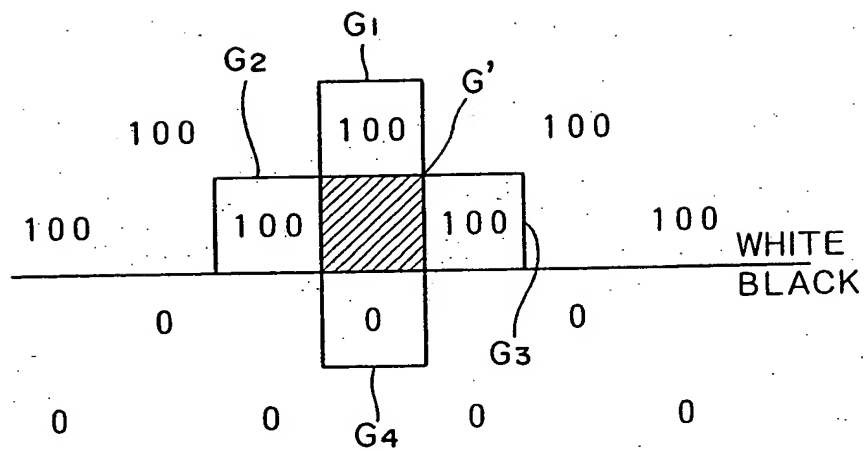
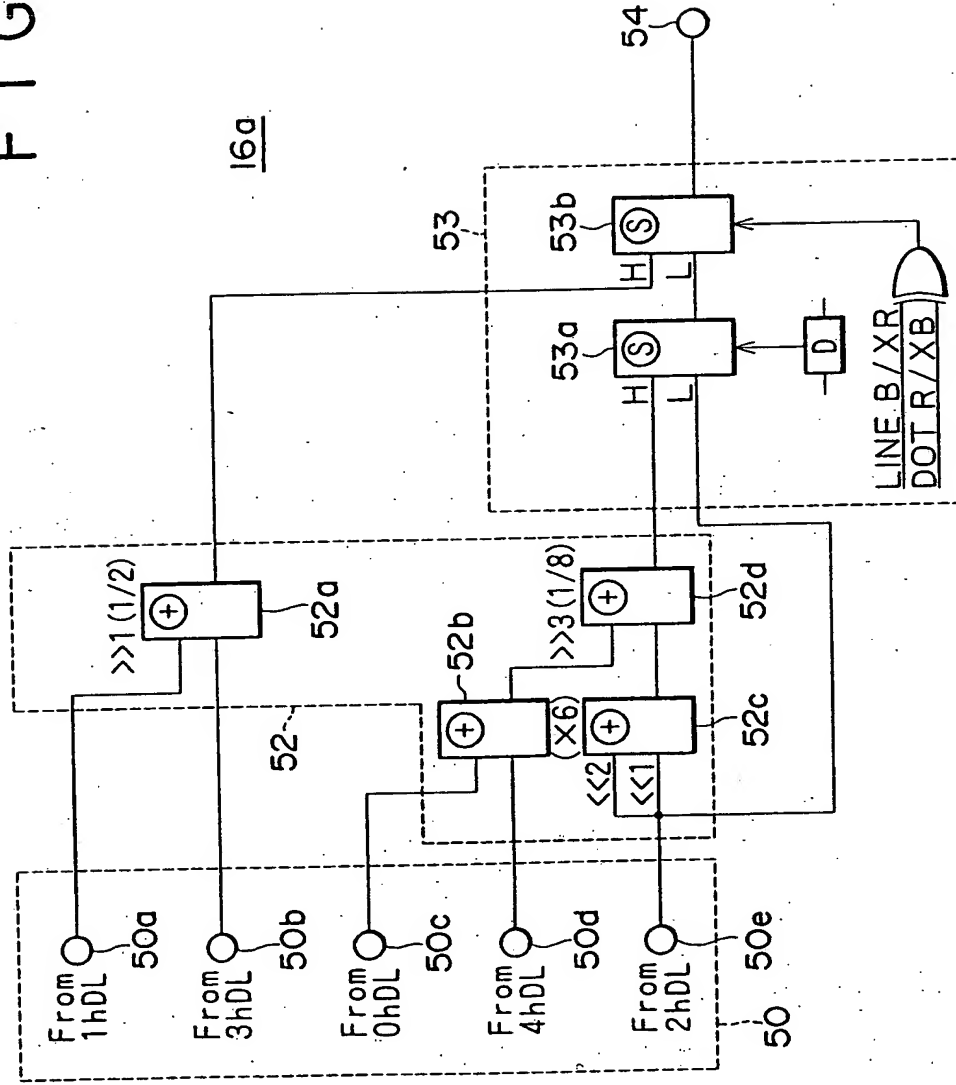


FIG. 15



EXAMPLE OF EDGE PROCESSING

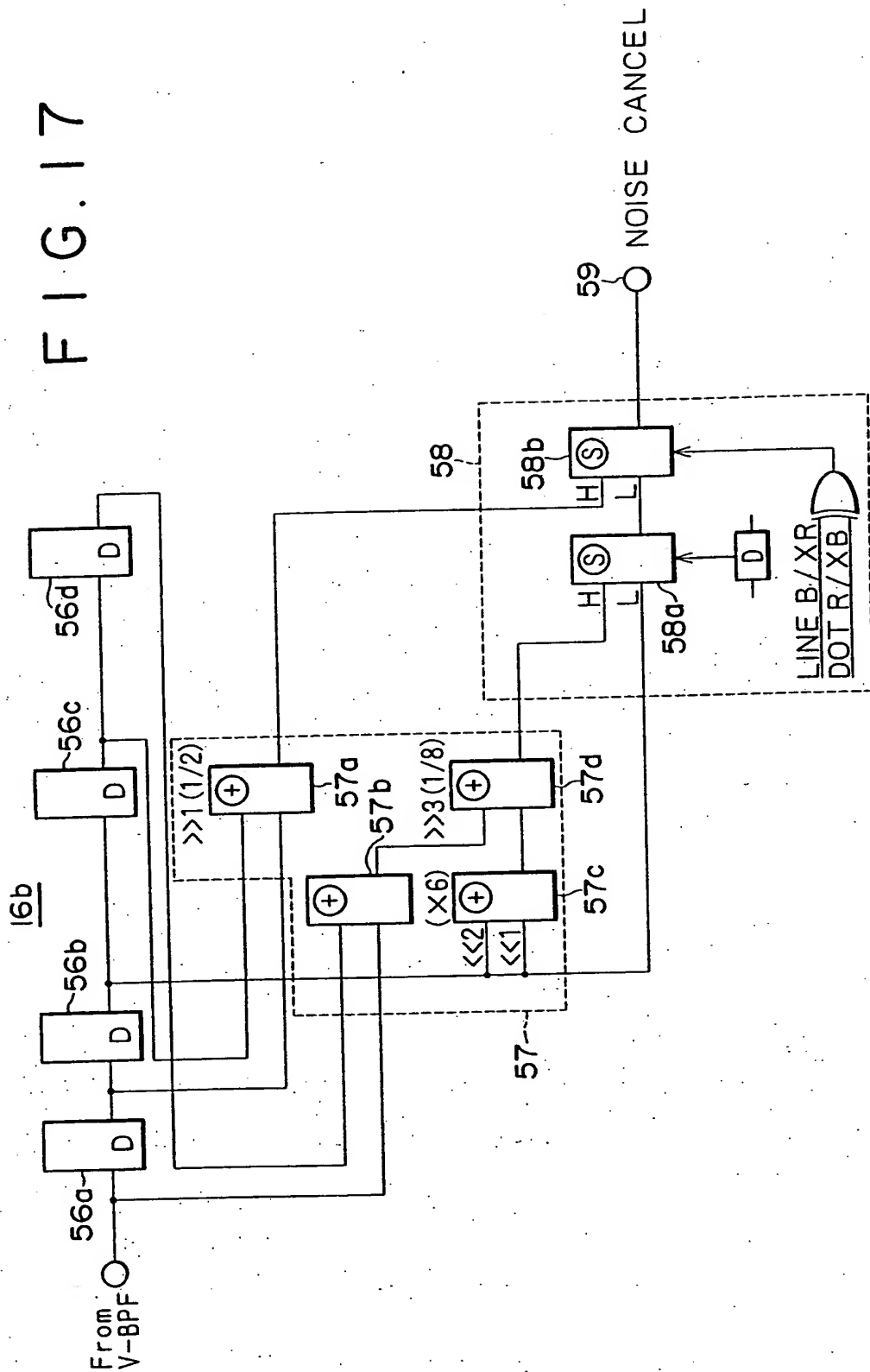
FIG. 16



CONSTITUTION OF HORIZONTAL-DIRECTION CORRELATION DETECTOR

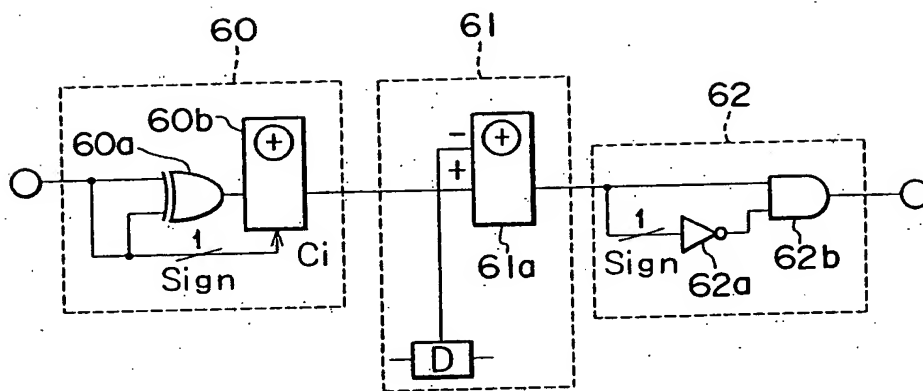


FIG. 17



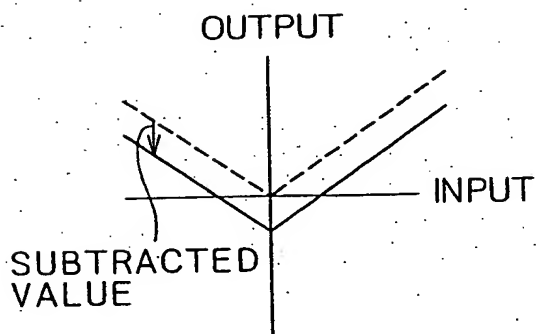
CONSTITUTION OF VERTICAL-DIRECTION CORRELATION DETECTOR

# FIG. 18

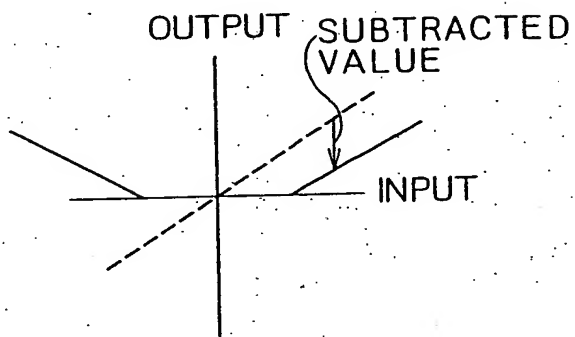


CONSTITUTION OF NOISE CANCELER

## FIG. 19A



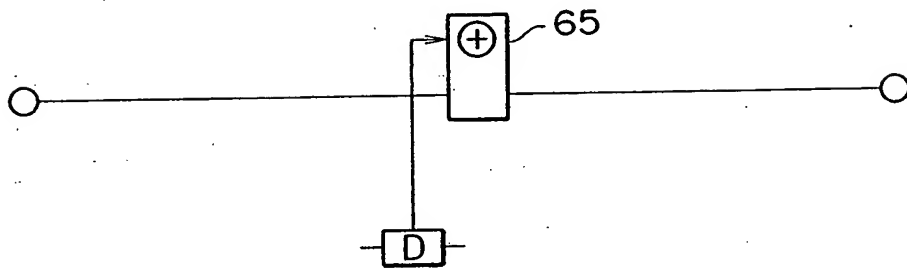
## FIG. 19B



PROCESSING OF CORRELATION VALUE

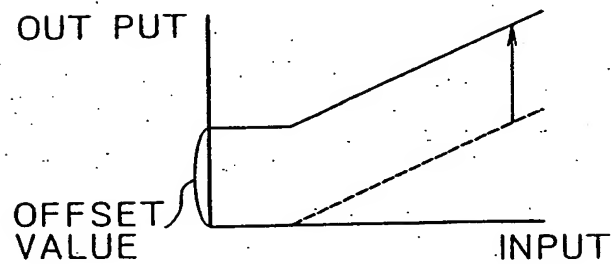
FIG. 20

18a, 18b



CONSTITUTION OF OFFSET CIRCUIT

FIG. 21



INPUT/OUTPUT CHARACTERISTIC

FIG. 22

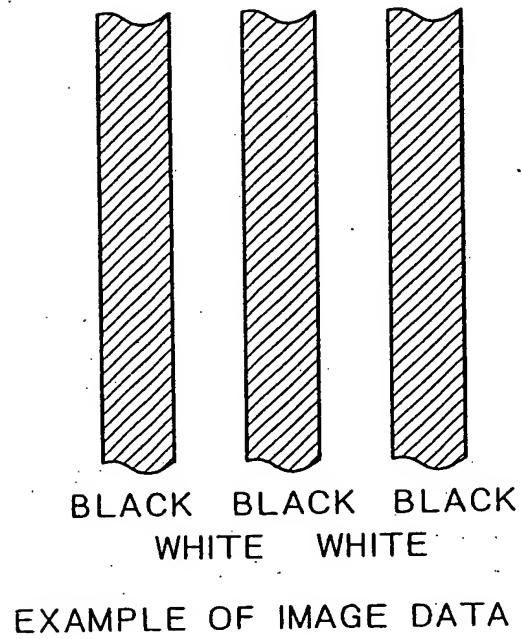
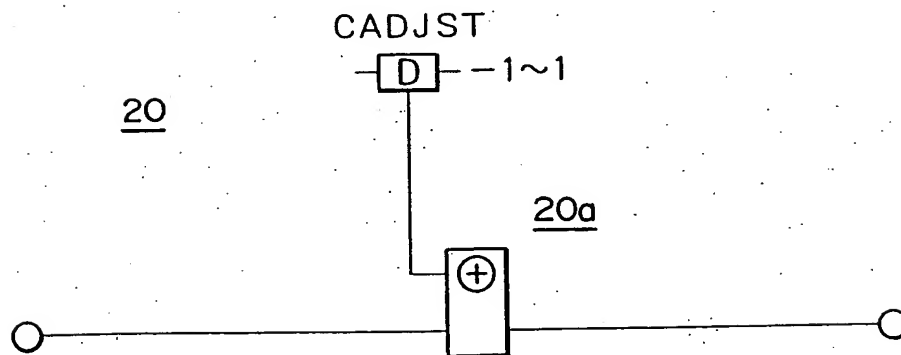
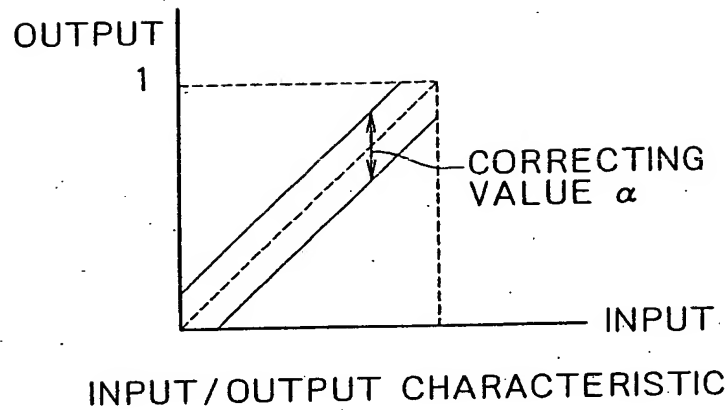


FIG. 23

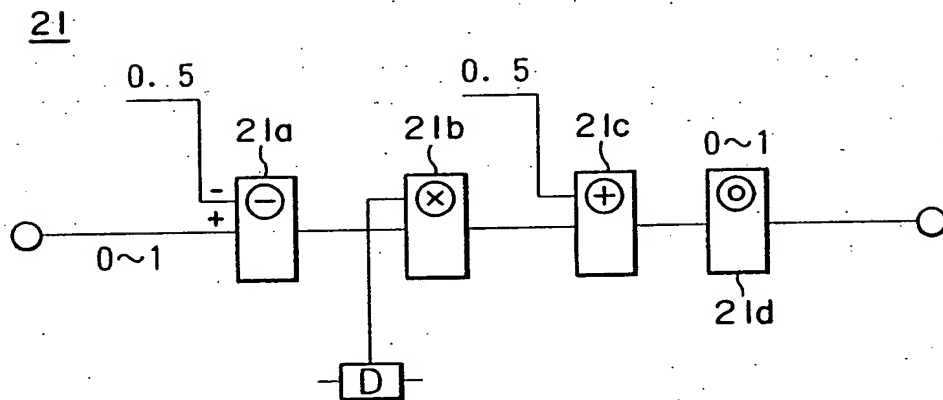


CONSTITUTION OF BIAS CORRECTING CIRCUIT

# FIG. 24

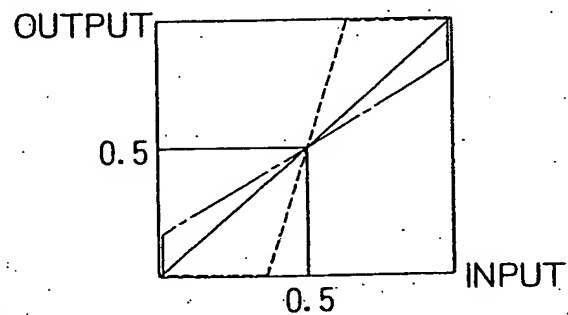


# FIG. 25

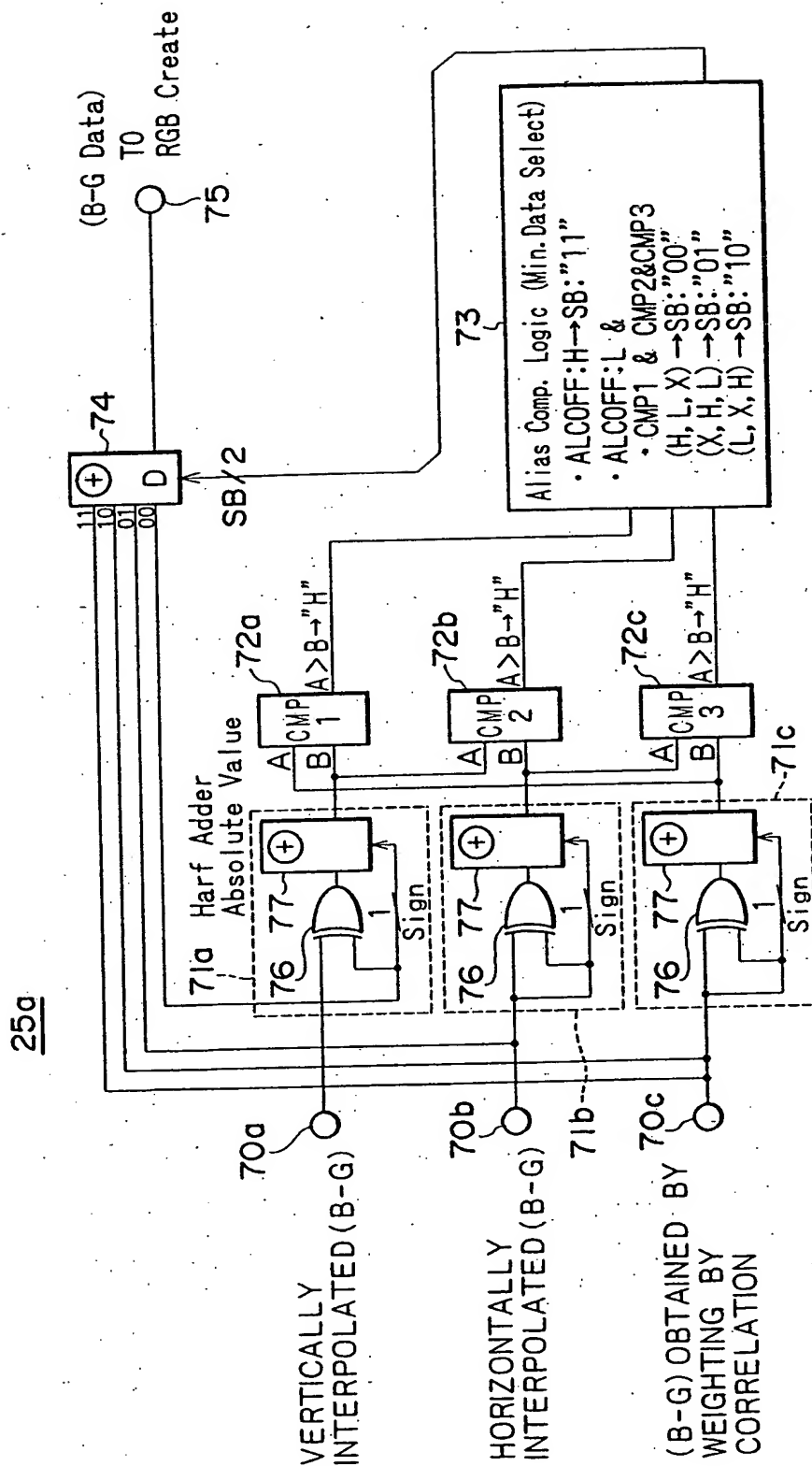


CONSTITUTION OF EMPHASIS/DEEMPHASIS CIRCUIT

# FIG. 26



# FIG. 27



CONSTITUTION OF COLOR-DIFFERENCE SIGNAL SUPPRESSER

FIG. 28A

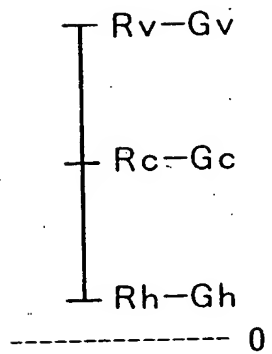
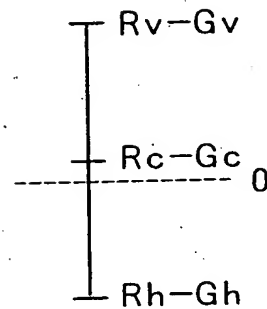


FIG. 28B



EXAMPLE OF SELECTING MINIMUM  
INTERPOLATED PIXEL DATA

FIG. 29A

G	R	
B	G	

FIG. 29B

G	Ye	
Cy	G	

ARRANGEMENT OF PIXEL DATA